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## Asynchronous DSPs: Low power, high performance

**An asynchronous DSP offers better power, performance, and reliability than one based on standard synchronous logic. It also enables simpler and less expensive PCB and power supplies.**

By James Awad, Octasic

For a useful primer on circuit design, see [Optimize your DSPs for power and performance](#). To learn how power and performance vary with voltage and temperature, see [Push performance and power beyond the data sheet](#).

Until today, the performance of a processor has primarily been measured by the speed of its clock. The vast majority of integrated circuit (IC) designs have been based on a [synchronous](#) architecture, which is governed by a global clock. This architecture has become so ubiquitous that it is considered by many to be the only way to design digital circuits. There is, however, an altogether different design technique that is just now coming to the forefront: [asynchronous](#) design.

The main driver for this is the state of silicon technologies. As silicon geometries shrink below 90 nanometers, power reduction has become the top priority. Because asynchronous design offers lower power and more reliable circuits, it has been proposed as a way to address this requirement.

Asynchronous design has been avoided in the past for many reasons, the most important being the lack of a standardized tool flow. To deliver devices quickly, IC design teams use high-level programming languages in combination with electronic design automation (EDA) tools that speed tasks such as logic design. If such tools were available for asynchronous design, we would likely see more devices with asynchronous logic components.

In the past, most asynchronous designs were small circuits used to complement synchronous circuits. Larger asynchronous devices have appeared recently, but these devices often targeted niche markets such as embedded sensors.

We believe that the opportunities for asynchronous logic are far greater than past devices suggest. In this article we make the case for a general purpose digital signal processor (DSP) core based entirely on asynchronous logic. We reveal many benefits, both for the IC designer and the end user.

### Synchronous vs. Asynchronous

Synchronous design is the de facto technique for digital design today. This methodology has been highly refined and the design tools are highly evolved. Synchronous design offers a standard flow—based on high-level languages—that enables rapid development. Synchronous design also provides an easy way to scale performance. Designers can create faster versions of a design by simply increasing the clock frequency.

Synchronous logic is broken down into asynchronous logic stages surrounded by [flip-flops](#) (also known as latches). These stages perform operations and pass the result on to the next stage. Figure 1 presents a simplified model of a single stage. The flip-flops store the current state associated with the logic. When a clock signal arrives, the flip-flops update their values, allowing new data to enter the logic. The asynchronous logic then calculates the new state of the circuit. For example, the logic cloud could perform an addition or multiplication.

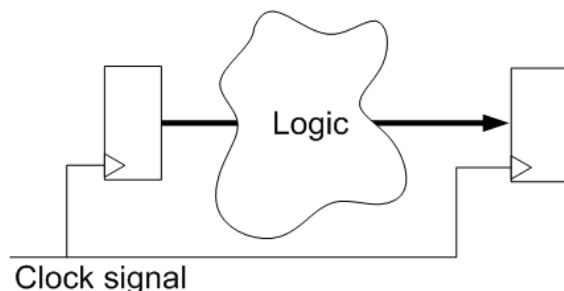


Figure 1. Simplified diagram of a synchronous logic stage

In an asynchronous circuit, the logic stages are modified to remove the clock. The basic building block for this architecture is shown in the Figure 2. Instead of a clock controlling the latches, the logic stage provides a completion signal to let the following logic stage know that a new output is ready. The timing of the completion signal depends on the specific operation of the logic. For example, the logic may be able to achieve [early completion](#) for certain combinations of input signals.

### The Benefits of Asynchronous Design

The benefits of asynchronous DSP are quite compelling. When used correctly, asynchronous design can

This local delay control is the reason for the robustness of asynchronous circuits. Since the logic controlling timing is near the computational logic, it will match the computational logic's response to changes in voltage, process speed and temperature.

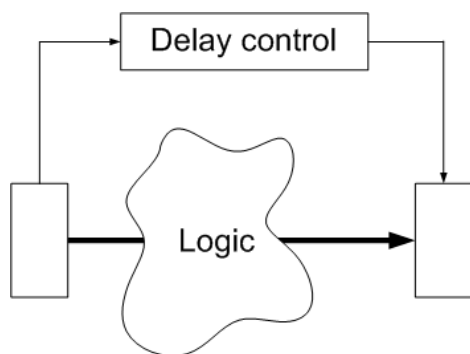


Figure 2. Simplified diagram of an asynchronous logic stage

There are many different approaches to asynchronous design, but the main theme is that the circuit is not governed by a single clock. Asynchronous logic is often used to solve specific problems with specific circuit designs. However, it is possible to use asynchronous logic as the basis for a complete DSP core.

provide lower power consumption, low electromagnetic interference (EMI), and can even simplify designs because it eliminates global clock skew.

#### Lower Power Consumption

The most important benefit of an asynchronous DSP versus a synchronous DSP core is its lower power consumption. In fact, Octasic's [Opus](#) asynchronous DSP core has been shown to be an order of magnitude more power efficient than the leading synchronous DSPs.

The issue of power consumption is becoming more and more relevant as silicon geometries shrink. Digital designers have managed to work around this problem thus far by reducing voltage. However, [threshold voltage](#) limitations mean that voltage can no longer decrease substantially using current semiconductor technologies.

In CMOS technologies, energy is consumed when gates switch states. In synchronous circuits, the need for a clock creates a lot of switching and therefore power consumption. Distributing a clock throughout a device or region of a device requires clock buffers. These clock buffers must be large to ensure that [skew](#) is minimized. In other words, all points in the circuit must see the clock transition at the same time. [Clock distribution](#), often called a clock tree, typically consumes almost half of the total system power. The clock buffers at the root of the tree have a very large [fanout](#) and are quite large, and therefore consume a lot of power.

Many techniques have been developed to counter this power consumption, such as clock gating. To date, none of these techniques are able to achieve the lower power consumption of an asynchronous design.

Clock gating is not required for an asynchronous circuit. In fact, an asynchronous circuit only consumes power when it is performing useful operations. In other words, the power consumed by an asynchronous circuit scales according to the performance delivered. In addition, this means that an asynchronous device has inherently low standby current.

#### Better Switching Performance

In addition to providing low power consumption, asynchronous logic offers very low EMI. This has many benefits, both for the IC designer and the end user.

As we noted earlier, synchronous circuits require global (or at least regional) clock signals. These clocks are the single largest contributor to EMI. Because the clock needs to switch everywhere at the same time, the EMI emitted by a synchronous device has pronounced peaks at specific frequencies.

EMI noise created by high-speed devices gets onto power planes of the PCB. This noise then appears on external I/Os or cabling, causing unwanted and often unpermitted radiation through wires. Decoupling capacitors are used as a first line of defense, whereas more expensive shielding or common-mode chokes are used as a last resort.

EMI on the power planes also complicates design of the power supplies. For synchronous circuits operating at high speeds, the power supplies must be filtered or over-margined to account for the voltage spikes created on the power planes.

[Ed: For an in-depth look at these topics, see [Avoiding noise and EMI problems in DSP systems](#).]

These noise and power supply issues add up to headaches for system designers, especially when using many high-speed DSPs in a given design. These problems are alleviated or eliminated by an asynchronous logic design. In asynchronous logic, the lack of global clocks cuts EMI dramatically. This makes PCB design much easier, and increases system reliability.

Asynchronous designs also have much lower power ripple, which simplifies power supply design. Figures 3 and 4 demonstrate the difference in power plane noise between a synchronous and an asynchronous DSP.

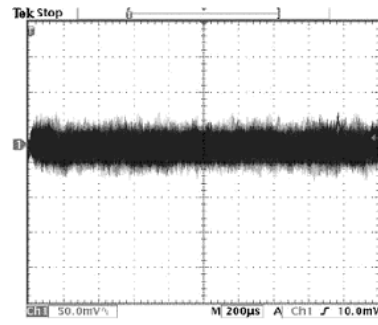


Figure 3. Synchronous DSP voltage ripple

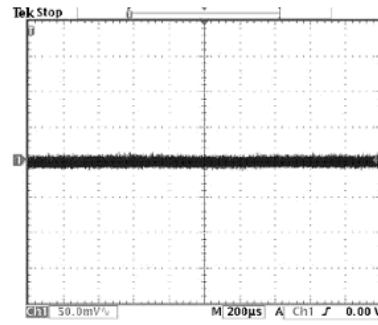


Figure 4. Asynchronous DSP voltage ripple

From the IC designer's point of view, this better switching performance means more reliable circuits. When large portions of a circuit switch at the same time, there is a large instantaneous current draw. This is observed on the power grid of the device as an IR-drop. This means that a region of the power grid is at a lower voltage momentarily. The designer must ensure that the power grid can sustain this drop in voltage. Sometimes this is the limiting factor that prevents a designer from doing more with a given region of logic.

#### Eliminating Clock Skew

There are other reasons to adopt asynchronous design. Silicon produced at sub-90 nm is very prone to fabrication issues. This is evidenced by the enormous effort spent by silicon manufacturers to correct for these problems. They've begun developing advanced techniques such as interferometric metrology, which tries to account for the fact that minimum feature sizes on the photomasks are now smaller than the exposure wavelength.

Controlling these variations in process is important because variations increase the skew across a device. Clock skew is defined as the difference between the arrival times of the clock signal at different points in the circuit. Since all logic on the same clock must operate coherently, skew must be kept to a minimum to ensure the circuit operates correctly. The faster the clock rate of the device, the less skew can be tolerated.

As feature sizes shrink, skew becomes a much bigger issue. Whereas previously, we would see "slow" chips and "fast" chips from a given wafer, we now see these variations across a single chip since the density has increased so much. This type of situation can be lethal for large monolithic synchronous devices.

An asynchronous DSP core avoids these problems altogether. The DSP core is built up of small self-timed circuits. Therefore all timing is local to the small area related to this block of logic.

#### Improved Robustness

Semiconductors are affected by three main physical properties: fabrication process speed, power supply voltage level and temperature. Each of these characteristics, if varied, will cause a transistor to operate faster or slower.

[Ed: To learn more about these variations, see [Push performance and power beyond the data sheet.](#)]

In the case of synchronous circuits, static timing analysis must be performed at the best- and worst-case values of all these parameters in order to ensure that the device will be functional across its entire range. In other words, with a synchronous circuit, there is a "cut-off point" where the circuit stops working.

Asynchronous circuits are self-timed, so they simply speed up or slow down as the physical characteristics vary. Because the logic that manages the self-timing is located in the same area as the processing logic, they are both affected by the same environmental changes of temperature and voltage. As a result, an asynchronous circuit is much more impervious to transient changes such as dynamic voltage drop, and can automatically self-adjust to long-term temperature and voltage changes.

#### The Debut: General Purpose Asynchronous DSPs

Until recently, asynchronous circuits were only used when absolutely necessary. They were considered to be on the fringe, usually restricted to academia. However, many commercial devices have exploited the benefits explained above in various niche markets. The recent success of these designs has sparked renewed interest in the technology.

The appearance of a general-purpose DSP core built completely from asynchronous logic indicates that the

tools, techniques and knowledge exist to create commercial products that can reach a broader audience. What's more impressive is that this device can be programmed and operates just like any off-the-shelf DSP. In other words, this solution provides all the benefits of asynchronous technology without any of the feared compromises in terms of usability.

#### About Octasic

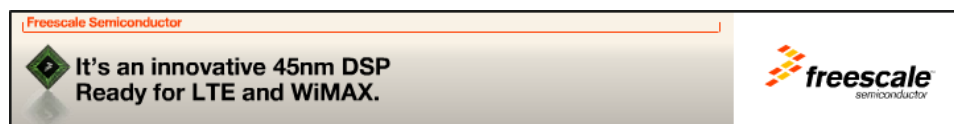
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#### About the Author

James Awad is a product marketing manager at Octasic Semiconductor and has more than nine years of experience in telecommunications. He received his bachelor's degree from Concordia University in Montreal, and has a strong background in ASIC design and system architecture for Voice-over-Packet networks. While at Octasic, he has developed expertise in echo cancellation and voice quality.

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