

The OCT2224M System-on-Chip devices are very low-power, high-performance multi-core DSPs, coupled with an optional ARM11 processor and a complete software development suite.

### OCT2224M Features

#### High-performance Multi-core DSP

- 24 Opus2 DSP cores
- C programmable DSP

#### ARM1176JZ-S Application Processor

- 500-MHz clock rate
- Support for 32-bit and 16-bit (Thumb® Mode) instructions

#### Characteristics

- 484-Pin Ball Grid Array (BGA) package, 1.0mm pitch
- 3W typical power consumption

#### On-chip Functions

- Fully secure custom booting capability
- Clock Synchronization Unit

#### Peripheral Interfaces

- One 4x (or two 1x) Serial RapidIO Links, v1.3 compliant
- One 1x PCIe link 2.5 Gbps, v1.1 or v2 compliant
- Four Ethernet MACs with parallel and SGMII modes
- 3 Parallel Interface (PIF) ports. Supported protocols include:
  - Multiple BT.656 & B.1120 video capture/display
  - Generic parallel interface to FPGA
- USB 2.0 ULPI Interface. High-/Full-Speed Host
- Flexible TDM interface
- Flash memory interfaces for ONFI NAND or Serial NOR Flash
- DSP Debug port
- 2 UARTs
- Configurable SPI, SSP, microwire serial port
- General Purpose I/Os (GPIO) pins
- IEEE-1149.1 (JTAG™) Boundary Scan Compatible
- 32-bit DDR2/3 Memory interface

### OCT2224M Benefits

- A single family of devices can be used for many applications across a broad range of capacities
- Lowest power fixed point DSP in the industry
- SoC architecture offers the most cost-effective solution available
- GUI based software development environment

### OCT2224M Target Applications

- Gateways (Wireline & Wireless)
- IP PBX
- Audio/Video transcoding gateways
- High-Definition (HD) Video conferencing
- Video Surveillance Digital Video Recorders (DVRs)
- Medical Imaging

### Development Tools

Octasic offers a complete set of development tools for the OCT2224M devices. *Opus Studio*, an integrated development environment (IDE), provides the necessary tools for code editing, compiling, simulation, debugging, and profiling. Octasic also provides a real-time kernel and RTOS services upon which embedded applications can rapidly be developed.

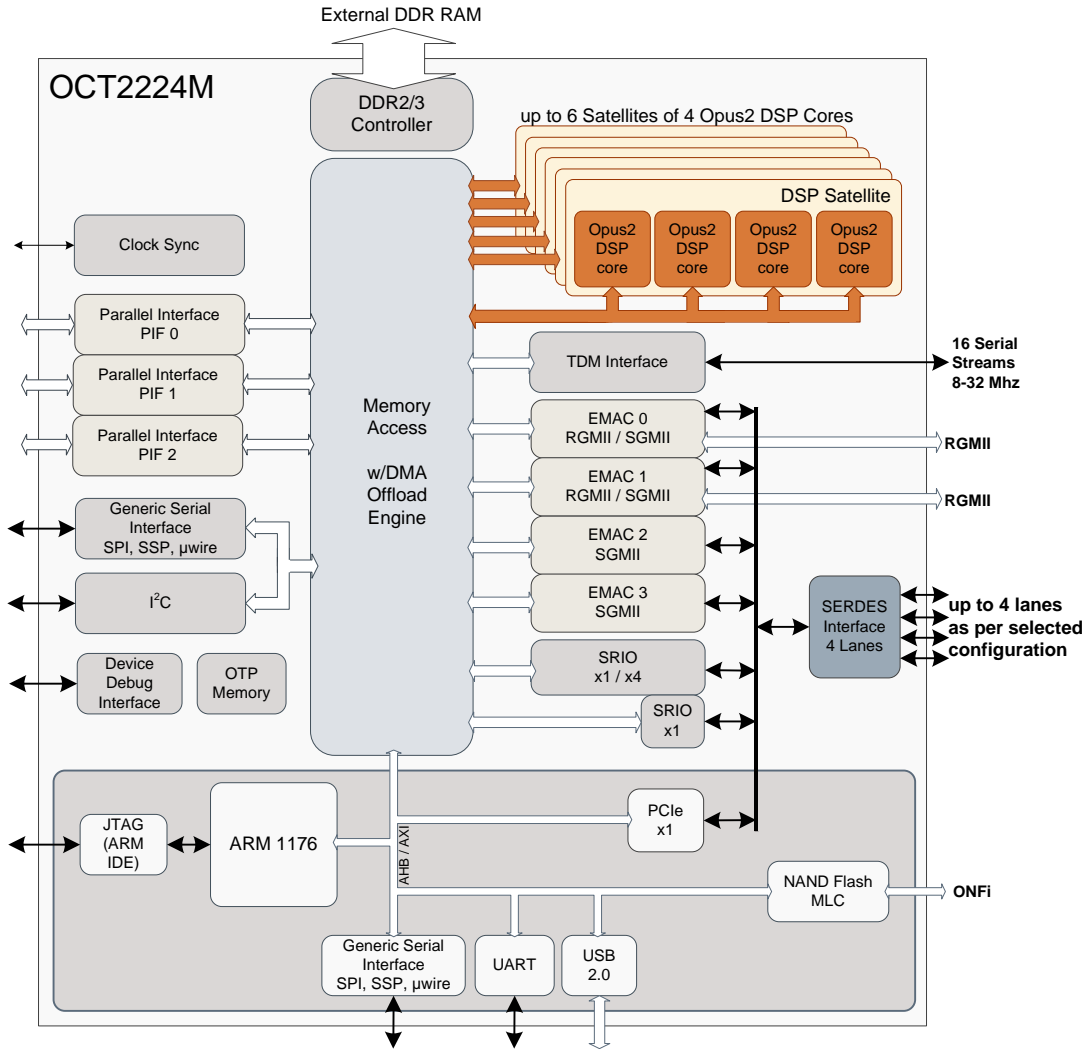
Octasic provides hardware development platforms to evaluate performance and begin development.

### Package Description

484-Pin Ball Grid Array (BGA)

Dimensions: 23mm x 23mm x 1.0mm pitch

PRELIMINARY

**OCT2224M Block Diagram**


PRELIMINARY

**OCT2224M Hardware Description**

The OCT2224M is composed of 24 Opus2 DSP Cores. The DMA subsystem provides a high-bandwidth interconnect between the cores, peripherals, and external memory.

**Opus2 DSP Processor Subsystem**
**Opus2 DSP Core**

The OCT2224M is composed of up to 24 Opus2 cores. Opus2 is a low-power, high-performance DSP core. The Opus2 core offers the following features:

- 144K bytes of L1 memory per core
- Rich instruction set

**Opus2 DSP Satellite**

The OCT2224M includes up to six satellites, each of which is composed of four Opus2 DSP Cores. A satellite has its own local bus and DMA. Data transfers can be local to the satellite or global.

**ARM Subsystem**
**ARM1176JZ-S Application Processor**

- 500-MHz clock rate
- Support for 32-bit and 16-bit (Thumb® Mode) instructions
- Embedded ICE-RT Logic for Real-Time debugging
- ARM® Jazelle® Technology
- Embedded Trace Macrocell (ETM)
- Embedded Trace Buffer (ETB) with 4KB memory
- ARM11 memory architecture
  - 16K-byte Instruction cache
  - 16K-byte Data cache
  - 16K-byte Instruction Tightly Coupled Memory (ITCM)
  - 64K-byte Data Tightly Coupled Memory (DTCM)

## DDR2/DDR3 Memory Subsystem

### Direct Memory Access (DMA)

The DMA controller connects all cores and peripherals to each other and to external memory.

The DMA provides 40 Gbps of bandwidth. This advanced DMA controller provides application-specific modes such as multi-dimensional transfers for video applications and high-speed core-to-core and multi-cast transfers.

### DDR2 /DDR3 Controller

Support is provided for both DDR2 and DDR3 memory devices.

- 32-bit data bus width
- DDR2-667 or DDR3-667
- Can address up to 2Gbytes total memory

Typical systems use two 16-bit wide memories.

## OCT2224M Peripheral Interfaces

### TDM Interface

The TDM Interface provides the following capabilities:

- 16 data streams can be individually configured as input or output.
- Supports a wide range of data rates: 2.048 Mbps, 4.096 Mbps, 8.192 Mbps, 16.384 Mbps.
- Supports up to 4096 timeslots.
- Programmable data sampling point for long TDM buses.
- Wide range of frame synchronization signaling.
- Supports Master and Slave clocking modes.

### Generic Serial Interface (GSI)

The GSI interface supports multiple industry standard serial interfaces such as SSP, SPI and Microwire.

Bit rates up to 3.4 Mb/s are supported.

### I<sup>2</sup>C Interface

The interface supports both master and slave modes.

### Ethernet MAC Engines

OCT2224M MGW supports 10/100/1000-Mbps data transfer rates.

- Supports both full-duplex and half-duplex operation:
  - Half-duplex: Supports Carrier Sense Multiple Access with Collision Detection (CSMA/CD)
  - Full-duplex: Supports IEEE 802.3x flow control
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 KB
- Supports a variety of flexible address filtering modes
- Supports IEEE 802.1Q VLAN tag detection for received frames
- Complete network statistics with RMON/MIB counters (RFC 2819 / RFC 2665)
- 40MHz Station Management Interface (SMA or MDIO)

### Serial RapidIO

The Serial RapidIO interface can be used as one 4x link or as two 1x links. The interface is v1.3 compliant. Each link supports rates of 1.25-, 2.5-, or 3.125-Gbps.

### PCI Express (PCIe)

The OCT2224M supports connections to a PCIe backplane or switch via the integrated master/slave bus interface. The interface complies with *PCI Express Base Specification Revision 1.1*.

The PCIe interface provides 1 lane, at a maximum speed of 2.5Gbps. The OCT2224M can be configured as a Root Complex (Host) or as an Endpoint (Device) with a DMA engine.

### Selecting High-speed interfaces

The PCIe, Serial RapidIO and Ethernet interfaces are multiplexed onto 4 SERDES pairs. The following table provides the supported combinations.

Mode	Port 0	Port 1	Port 2	Port 3
0	SGMII/GMII/RGMII/MII/RMII	SGMII/RGMII/RMII	SGMII	SGMII
1	PCIe	SGMII	SGMII/SRIO (1.25G)	SGMII/SRIO (2.5G)
2	SGMII	SGMII	SRIO (3.125G)	SRIO (3.125G)
3	SRIO x4 (3.125G x4)			

### Parallel Interface Port (PIF)

There are 3 parallel interface (PIF) ports on the OCT2224M. Each PIF port provides the following functions:

- Half and full-duplex communication
- 8 and 16-bit data interface
- Circular-buffer hardware allows low overhead continuous data streaming
- Source synchronous clocking and framing for Tx and Rx
- Maximum speed of 150 MHz

These three ports can be used independently, or PIF 0 and PIF 1 can be combined to achieve larger bit-widths or higher throughput.

PIF 0 and PIF 1 support Single Data Rate (SDR) and Double Data Rate (DDR) data latching. PIF 2 supports only DDR data latching. The PIF port was designed to support many different protocols.

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## OCT2224M Peripheral Interfaces (continued)

### Parallel Interface Port – Video

The PIF can be adapted to standard video capture and display interfaces such as ITU-R BT.656 / BT.1120. These standards operate using SDR signaling, therefore only PIF 0 and PIF 1 can be used.

The PIF ports support multiplexed streams. For BT.656, up to four 27 MHz streams can be multiplexed into a 108 MHz stream. For BT.1120, up to two 74.5 MHz streams can be multiplexed into a 148.5 MHz stream.

By combining PIF 0 and PIF 1, one 10-bit port can be supported instead of two 8-bit ports.

### Parallel Interface Port - Generic

Besides the standard video modes, the PIF can directly connect to many industry-standard video analog-to-digital (A/D) and digital-to-analog (D/A) devices.

The PIF can also be used to connect to an external FPGA or any other device through its synchronous parallel interface.

### USB Interface

The USB interface is compliant with the *Universal Serial Bus Revision 2.0 Specification*. The device supports Low-Speed, High-Speed and Full-speed Host mode, providing up to 480 Mbps.

The OCT2224M supports a UTMI+ low-pin interface (ULPI). This interface provides for a low cost means of connecting to off-the-shelf Hi-Speed USB transceivers.

### Flash Memory Interface

The OCT2224M supports either ONFI NAND or Serial flash.

### Boot

The OCT2224M provides a very flexible boot mechanism through the Ethernet, PCI, NAND, NOR, or SPI interfaces. It supports secure boot for decryption code and keys utilizing internal storage.

### Debug Port

The debug port is used to connect to and debug the Opus2 DSP cores. This port is used for hardware validation and initial boot-up.

## OCT2224M DC Electrical Characteristics

### Absolute Maximum Ratings

Operation beyond these limits may cause permanent device damage. All parameters representing voltages are measured with respect to ground.

Parameter	Min.	Max.
Core DC supply voltage	-0.5V	1.27V
1.8 V DC supply voltage	-0.5V	2.0V
2.5 V DC supply voltage	-0.2V	3.0V
3.3 V DC supply voltage	-0.5V	4.0V
Storage temperature range	-40°C	+125°C

### Recommended Operating Conditions

For normal device operation, adhere to the limits in the table below. Operation beyond these limits may impair the useful life of the device.

Parameter	Min.	Typ.	Max.
Core DC supply voltage		1.0-1.16V	
1.8V I/O DC supply voltage		1.8V	
2.5V I/O DC supply voltage		2.5V	
3.3V I/O DC supply voltage		3.3V	

## Ordering Information

### OCT22CCME-PIA

CC	Number of cores
M	Media processing device
E	RoHS lead-free indicator
P	Package type indicator
I	I/O configuration indicator
A	ARM processor indicator

Contact your Octasic sales representative for more information.

# OCT2224M



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