

Octasic's new GSM/HSPA+ Small Cell Basestation solution achieves the industry's highest user capacity and largest cell size in a single device for indoor Enterprise Femtocell and for outdoor Picocell and Microcell. By adding an HSPA+ Physical Layer (PHY) to Octasic's previously-released GSM/EDGE solution based on the OCT2224W System on a Chip (SoC), the Small Cell can run GSM and HSPA+ air interfaces concurrently thanks to the SoC's multi-core Opus2 DSP.

System Features

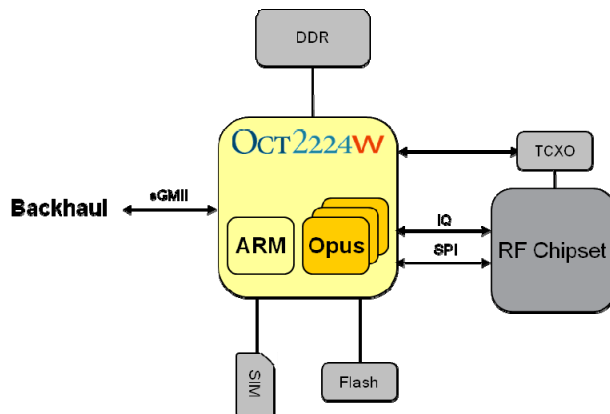
- Complete 3GPP Release 8 WCDMA/HSPA+ Basestation
- 42 Mbps downlink, 11 Mbps uplink
- Receive Diversity
- Transmit MIMO
- Up to 64 active users
- UE speed up to 250 km/h
- Encryption in software on Opus2: IPSec, AES, Kasumi
- Layer 2 in software on Opus2: MAC, RLC, PDCP
- Support for lub, luh, FAPI, Abis, FRMI

Benefits

- Single device offers Enterprise Femtocell, Picocell, or Microcell solution
- High Capacity - up to 64 active users
- Designed for indoor/outdoor BTS
- Cell radius up to 50 km
- SoC runs all 3GPP PHYs available from Octasic
 - GSM, EDGE, WCDMA, HSPA+, LTE (upcoming)
 - Concurrent multi-PHY operation
- Lowest power fixed point DSP in the industry
- SoC architecture offers the most cost-effective BOM

HSPA+ Small Cell Platform

The SoC integrates processing and system functions with a rich set of interfaces to enable system designers to build small cell base stations with fewer components and a reduced BOM.

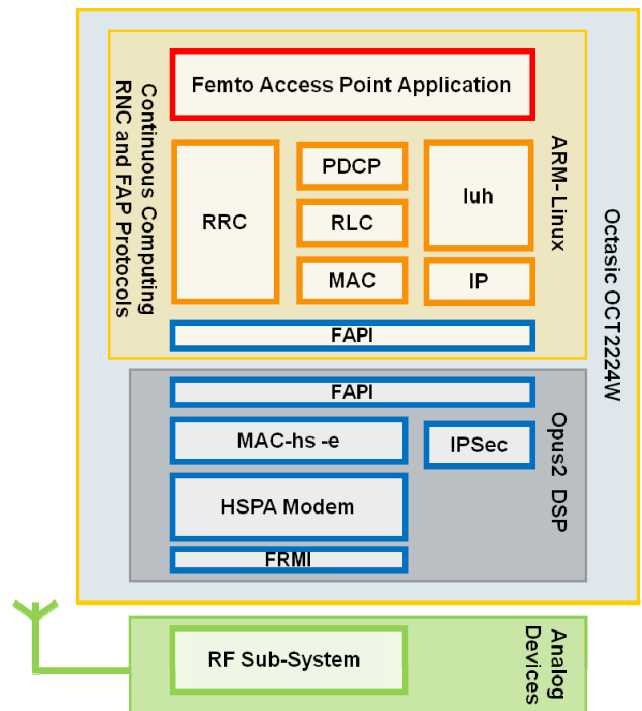


The solution integrates the complete signal and packet processing required to convert IQ radio samples from the RF front end to IP packets on the backhaul interface. It also embeds system functions such as precise timing control and OTP with multiple radio and backhaul interfaces.

The Opus2 multi-core programmable architecture makes it possible for multiple air interfaces such as GSM, EDGE, and HSPA to run concurrently, each controlling their own RF Transceivers.

HSPA+ Software Architecture

The Octasic reference system integrates Continuous Computing FAP & RNC stacks with an HSPA+ PHY through a common API built on Femto Forum's FAPI interface. Encryption tasks are performed in software on Opus2 DSP. Layer 2 functions (MAC, RLC, PDCP) are also performed on Opus2 DSP for higher HSPA+ data capacity.



PRELIMINARY

OCT2224W System on a Chip Features

- ARM1176JZ-S 500MHz CPU for protocol stack
- Hardware Accelerator Block (HAB)
 - Fast Fourier Transform Accelerator (FFTA)
 - CDMA Search Engine (CSE)
 - Path Search and RACH Preamble Detection for W/CDMA standards
 - Channel Decoder Engine (CDE)
 - Support for Viterbi, Turbo, and CTC modes of all air interfaces
- Security
 - TrustZone
 - Secure boot
 - 32KB OTP fuses for keys, unique ID, custom boot
- Hardware support for packet-based timing
 - IEEE1588, NTP, GPS, Cell Sync
- 3.5 Watts Total Power
- Glueless interface to three independent RF front ends
 - 16-bit DAC/ADC in full-duplex or half-duplex mode
 - SISO, MISO, MIMO 2x2
 - Dedicated SPI and GPIO for RF control on each port
- Four Ethernet MACs
 - 10/100/1000Mbps MII, RMII, GMII, RGMII, SGMII
- USB, SIM, NAND Flash, and SDRAM interfaces
- Fully C-programmable architecture
 - Ability to customize Octasic PHYs
 - Proprietary PHY porting
- GUI-based software development environment with optimizing C compiler

PRELIMINARY

