The OCTBTS5000 is a dual-sector software defined base station platform that supports any combination of LTE, UMTS/HSPA, CDMA2000 or GSM sectors. The OCTBTS5000 is also a perfect platform for developing custom waveforms and implementing LTE Advance and 5G systems which require MIMO capability and demand high processing power. This single-width mid-size AMC module houses four Octasic DSPs, two NXP quad-core ARM CPUs and a powerful Xilinx FPGA. There are two Analog Devices AD9361 RF-SoCs on the RF interface card operating between 70Mhz and 6Ghz with up to 56Mhz analog bandwidth per channel. The OCTBTS5000 is also available with two SFP connectors on the front panel providing CPRI link and allowing the module to be used with third party remote radio head (RRH) solutions.

The OCTBTS5000 platform incorporates Octasic’s flexiPHY GSM, UMTS/HSPA, and LTE-FDD/ TDD software, and is pre-integrated with a range of commercial Layer 2/3 protocol stacks from leading vendors. OEMs can leverage the complete solution to deliver high-performance base stations offering their own differentiating features, while reducing development time, cost, and risk. OEMs also have the option to integrate their own Layer 2/3 stack, or to implement fully custom waveforms using Octasic’s Opus Studio development environment.

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The OCTBTS 5000 is developed in collaboration with N.A.T. GmbH.

**Applications**
- LTE-FDD/TDD eNodeB and Network in a Box
- LTE Advanced
- 5G Network Testing
- MIMO and Massive MIMO Applications
- GSM/GPRS/EDGE and UMTS/HSPA base stations
- Wireless Surveillance
- Custom Military Waveforms
- Public Safety and Mission-critical Applications

**Features**
- Four OCT2224W DSPs
- Xilinx Kintex-7 XC7K160T FPGA
- Two NXP LS1043A CPUs
- RF Interface Options:
  - Two AD9361 RF-SoCs
  - Two SFP connectors for CPRI links
- Supports up to:
  - 20 km range for 3G
  - > 50 km for LTE
  - 100/40 Mbps LTE throughput
  - 32 3G users
  - 32-128 LTE users
RF Interface
Two Analog Devices AD9361 RF-SoCs offer four Rx and Tx antenna ports operating between 70MHz and 6GHz with up to 56MHz analog bandwidth.
The RF interface is implemented on a mezzanine module, so it can be easily adapted to new technologies or different RF front ends.

Subsystem Processor
The on-board Xilinx Kintex-7 FPGA provides pre-DSP data manipulation as well as headroom for further extension and customization. This includes efficient linearization, i.e. using a single digital pre-distortion (DPD) per user instead of each power amplifier, and other data pre-processing capabilities.

PHY Processing Array
Four Octasic OCT2224W DSPs, each with 24 DSP cores, provide the specialized power needed for PHY processing. Each DSP is equipped with its own private external 512MB DDR3 memory.

L2/L3 and Core Processing
Two NXP QorIQ™ LS1043A processors for L2/L3 and core processing. These quad-core 64-bit ARM-based processors are each supported by 4GB DDR4 memory and feature a data path acceleration architecture.

Switching
A Broadcom BCM5396 device establishes a full-non-blocking interconnect between the DSPs, CPUs, FPGA and backplane and provides an individual data and control path access to these devices.

Clock Interfaces
A GPS antenna input on the front panel connects to on-board GPS receiver circuitry. The module also features an additional external reference clock input on the front panel, a TCLKA-D interface (receive or transmit) on the backplane connector and an on-board Stratum-3 oscillator.
Software Solution

Users of the OCTBTS 5000 have access to integrated hardware/software packages. DSPs run physical layer (PHY) software for multiple cellular standards including GSM/GPRS/EDGE, CDMA2000, UMTS/HSPA, LTE-FDD/TDD and radio utility system (RUS). RUS gives functionalities like Network Listen, RF Player/Recorder and Base station automatic synchronization. CPUs run higher layer protocol stack (Layer 2/3) and core network software for all cellular standards. All software layers (L1/2/3 and core) are fully integrated and can be delivered as a turn-key solution.

Complete SDR Development Environment

High Performance SDR Platform

The OCTBTS 5000 is a fully-programmable SDR base station platform. It supports standard cellular air interfaces, as well as proprietary waveforms, over a wide range of frequencies and channel bandwidths.

The OCTBTS 5000 offers a range of features designed to optimize the performance of base stations and radio systems, including:

- Each transceiver/baseband combination can be configured as an independent radio sector.
- Hardware acceleration blocks (HAB) in the OCT2224W SoCs.
- Frequency agility under software control from 70 MHz to 6 GHz, with a frequency tuning time of 25 micro-seconds.
- Support for vehicular-speed mobility with macro base station style channel estimation and Doppler frequency shift correction.

Development Environment

Octasic provides a complete set of development tools for customers wishing to integrate their own Layer 2/3 software, or develop their own PHY layer and waveform code, including:

- Opus Studio integrated development environment (IDE)
- OCTBTS Evaluation and Development Kit (hardware and software)
- OCT2224W board support package (drivers)
- Source code licenses for flexiPHY

If you are interested in custom SDR development on the OCTBTS 5000 platform, please contact Octasic for further details.
# OCTBTS 5000 Technical Description

## Transceiver Specifications
- **Number of simultaneous bands**: 2
- **MIMO Support**: 2 x 2 (each sector)
- **Duplexing**: TDD and FDD options available
- **Frequency of operation**: 70 MHz to 6 GHz (other options also available)
- **Tuning time**: 25 micro-seconds
- **Channel sizes**: up to 56 MHz
- **Airlink support**: GSM/EDGE, UMTS/HSPA, LTE - FDD/ TDD, and CDMA2000 standards, as well as custom waveforms
- **RF Compliance**: 36.104 (E-UTRA), 25.104 (UTRA)

## Digital Section Specifications
- **DSP**: Quad Octasic OCT2224W Baseband SoC
- **CPU**: Dual NXP LS 1043A
- **CPU Operating System**: Embedded Linux
- **Memory**: 4GB DDR4

## Environmental Conditions
- **Temperature (operating)**: 0ºC to +60ºC with forced air cooling
- **Temperature storage**: -40ºC to +85ºC
- **Relative Humidity**: 10% to 90% at +55ºC (non-condensing)

## Backplane Connectivity
- **Full AMC TCLKA-D connectivity**
- **XAUI 10GbE (or custom SerDes protocol) connectivity to Fat-Pipe-Region ports #4-7**
- **Dual 1GbE connectivity to ports #0 and #1**
- **CPRI or custom SerDes protocol to ports #2 and #3**

## Front Panel
- **Bi-colour status LEDs, one for each DSP, one for each CPU, two for application status**
- **PLL lock status LED**
- **4x SMP Rx, 4x SMP Tx RF connectors**
- **GPS antenna RF connector (SMP)**
- **Control connector to external power amplifier**

## Standard Compliance
- **AMC.0 R2.0, AMC.2, IMPI V1.5 & V2.0, HPM.1, CE, RoHS, EN61000, EN5022, EN55024**

## Power Consumption
- **45W typical**