

The OCT2224W System-on-Chip (SoC) devices are very low-power, high-performance multi-core DSPs optimized for rapid development of wireless applications, coupled with a complete software development suite.

OCT2224W Features

High-performance Multi-core DSP

- 24 Opus2 DSP cores
- C programmable DSP

Hardware Acceleration Blocks (HABs)

- 6 dynamically reconfigurable Hardware Acceleration Blocks (HABs)
- Each HAB can perform the following functions:
 - I/FFT, I/DFT, RACH, Search, Viterbi, Turbo, and CTC

Characteristics

- 484-Pin Ball Grid Array (BGA) package, 1.0mm pitch
- 4W typical power consumption

On-chip Functions

- Fully secure custom booting capability
- RF Transceiver Clock Synchronization Unit
- Clock Synchronization Unit

Peripheral Interfaces

- One 4x (or two 1x) Serial RapidIO Links, v1.3 compliant
- One 1x PCIe link 2.5 Gbps, v1.1 or v2 compliant
- Four Ethernet MACs with parallel and SGMII modes
- 3 Parallel Interface (PIF) ports. Supported protocols include:
 - JESD207 digital converter interface for RF transceivers can be combined in hardware for MIMO support
 - Generic parallel interface to FPGA
- USB 2.0 ULPI Interface. High-/Full-Speed HostFlexible TDM interface
- Flash memory interfaces for ONFI NAND or Serial NOR Flash
- DSP Debug port
- Universal Integrated Circuit Card (UICC) Smart Card interface
- One Universal Asynchronous Receiver/Transmitter (UART)
- One Generic Serial Interface (GSI)
- One Inter-Integrated Circuit (I²C) interface
- Configurable SPI, SSP, microwire serial port
- General Purpose I/Os (GPIO) pins
- IEEE-1149.1 (JTAGTM) Boundary Scan Compatible
- 32-bit DDR3 Memory interface

OCT2224W Benefits

- A single family of devices can be used for many applications across a broad range of capacities
- Lowest power fixed-point DSP in the industry
- SoC architecture offers the most cost-effective solution available
- Complete GUI-based software development environment

OCT2224W Target Applications

Base-stations of all sizes for all air interfaces:

- Femtocell, Small cell, Picocell, Microcell
- All flavors of 2G, 3G, and 4G air interfaces
- 3 simultaneous air interfaces
- Physical and MAC/Protocol layers

Development Tools

Octasic offers a complete set of development tools for the OCT2224W devices. *Opus Studio*, an integrated development environment (IDE), provides the necessary tools for code editing, compiling, simulation, debugging, and profiling. Octasic also provides a real-time kernel and RTOS services upon which embedded applications can rapidly be developed.

Octasic provides hardware development platforms to evaluate performance and begin development.

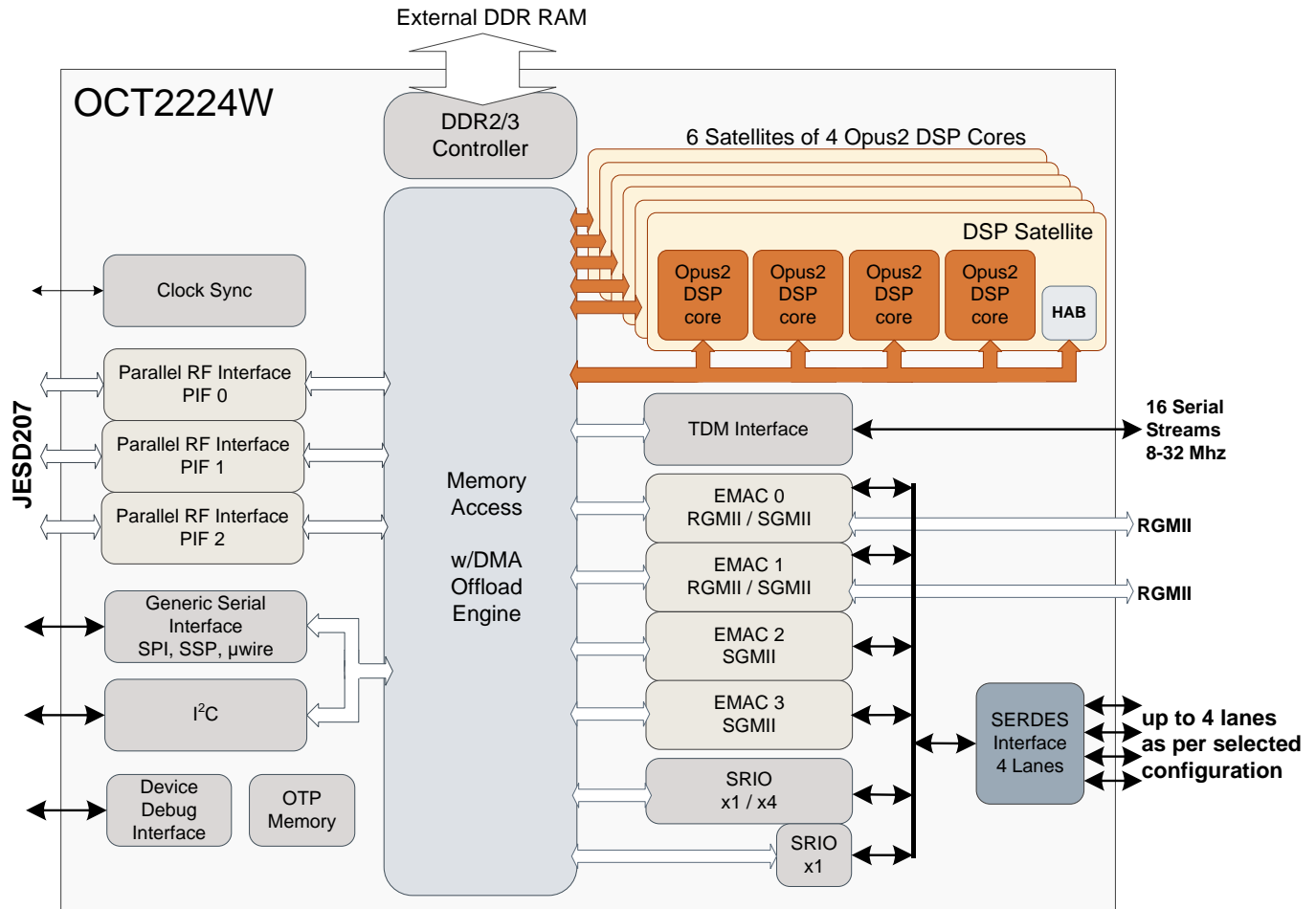
Package Description

484-Pin Ball Grid Array (BGA)

Dimensions: 23mm x 23mm x 1.0mm pitch

OCT2224W Block Diagram

The OCT2224W is composed of 24 Opus2 DSP Cores. The DMA subsystem provides a high-bandwidth interconnect between the cores, peripherals, and external memory.



Opus2 DSP Processor Subsystem

Opus2 DSP Core

The OCT2224W is composed of up to 24 Opus2 cores. Opus2 is a low-power, high-performance DSP core. The Opus2 core offers the following features:

- 144K bytes of L1 memory per core
- Rich instruction set

Opus2 DSP Satellite

The OCT2224W includes up to six DSP satellites, each of which is composed of four Opus2 DSP Cores and one Hardware Accelerator Block (HAB). Each satellite has its own local bus and DMA. Data transfers can be local to the satellite or global.

Hardware Accelerator Block (HAB)

The HAB is highly programmable and can be used sequentially for multiple functions with low task switching overhead. The HAB can perform the following specialized functions:

- Fast Fourier Transform Accelerator (FFTA)
 - I/FFT and I/DFT for OFDMA air interfaces
 - 64 to 2048 transforms
- CDMA Search Engine (CSE)
 - Path Search and RACH Preamble Detection for CDMA-based standards
 - 64 user, 150km, 2 antennas
- Channel Decoder Engine (CDE)
 - Supports Viterbi, Turbo and CTC modes of all air interfaces
 - Max of 12288 block size, rate 1/5, 16 state
- Fully micro-programmable processor with arbitrary feedback and generator polynomials

OCT2224W Peripheral Interfaces

TDM Interface

The TDM Interface provides the following capabilities:

- 16 data streams can be individually configured as input or output.
- Supports a wide range of data rates: 2.048 Mbps, 4.096 Mbps, 8.192 Mbps, 16.384 Mbps.
- Supports up to 4096 timeslots.
- Programmable data sampling point for long TDM buses.
- Wide range of frame synchronization signaling.
- Supports Master and Slave clocking modes.

Generic Serial Interface (GSI)

The GSI interface supports multiple industry standard serial interfaces such as SSP, SPI and Microwire.

Bit rates up to 3.4 Mb/s are supported.

I²C Interface

The interface supports both master and slave modes.

Ethernet MAC Engines

OCT2224W supports 10/100/1000-Mbps data transfer rates.

- Supports both full-duplex and half-duplex operation:
 - Half-duplex: Supports Carrier Sense Multiple Access with Collision Detection (CSMA/CD)
 - Full-duplex: Supports IEEE 802.3x flow control
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 KB
- Supports a variety of flexible address filtering modes
- Supports IEEE 802.1Q VLAN tag detection for received frames
- Complete network statistics with RMON/MIB counters (RFC 2819 / RFC 2665)
- 40MHz Station Management Interface (SMA or MDIO)

Serial RapidIO

The Serial RapidIO interface can be used as one 4x link or as two 1x links. The interface is v1.3 compliant. Each link supports rates of 1.25-, 2.5-, or 3.125-Gbps.

PCI Express (PCIe)

The OCT2224W supports connections to a PCIe backplane or switch via the integrated master/slave bus interface. The interface complies with *PCI Express Base Specification Revision 1.1*.

The PCIe interface provides 1 lane, at a maximum speed of 2.5Gbps. The OCT2224W can be configured as a Root Complex (Host) or as an Endpoint (Device) with a DMA engine.

Boot

The OCT2224W provides a very flexible boot mechanism through the Ethernet, PCI, NAND, NOR, or SPI interfaces. It supports secure boot for decryption code and keys utilizing internal storage.

Debug Port

The debug port is used to connect to and debug the Opus2 DSP cores. This port is used for hardware validation and initial boot-up.

Selecting High-speed interfaces

The PCIe, Serial RapidIO and Ethernet interfaces are multiplexed onto 4 SERDES pairs. The following table provides the supported combinations.

Mode	Port 0	Port 1	Port 2	Port 3
0	SGMII/GMII/RGMII/MII/RMII	SGMII/RGMII/RMII	SGMII	SGMII
1	PCIe	SGMII	SGMII/SRIO (1.25G)	SGMII/SRIO (2.5G)
2	SGMII	SGMII	SRIO (3.125G)	SRIO (3.125G)
3	SRIO x4 (3.125G x4)			

Parallel Interface Port (PIF)

There are 3 parallel interface (PIF) ports on the OCT2224W. Each PIF port provides the following functions:

- Half and full-duplex communication
- 8 and 16-bit data interface
- Circular-buffer hardware allows low overhead continuous data streaming
- Source synchronous clocking and framing for Tx and Rx
- Maximum speed of 150 MHz

These three ports can be used independently, or PIF 0 and PIF 1 can be combined to achieve larger bit-widths or higher throughput.

PIF 0 and PIF 1 support Single Data Rate (SDR) and Double Data Rate (DDR) data latching. PIF 2 supports only DDR data latching. The PIF port was designed to support many different protocols.

Parallel Interface Port – RF Interfaces

For wireless applications, the PIF ports can be configured as three independent Transceiver interfaces. These ports are compliant with JEDEC JESD207 (Radio Front-End Baseband Digital Parallel (RBDP) Interface).

Each port supports up to 16 bit ADCs and DACs. They function in half duplex mode (TDD) when 16 bit data Rx and Tx data is received/sent alternatively or in full duplex mode (FDD) when 8 bit data Rx and Tx are received/sent concurrently with MSB and LSB multiplexed in time.

For each port an SPI bus and 6 GPIOs are available to control the RF sub-system (Transceiver and Front End). Control signals can be implemented over either interface and synchronized with data by the hardware.

Ports 0 and 1 support 2 antennas in MIMO and MISO modes. To support higher data rate, Ports 0 and 1 can be bonded with common control signals to double data bandwidth.

USB Interface

The USB interface is compliant with the *Universal Serial Bus Revision 2.0 Specification*. The device supports Low-Speed, High-Speed and Full-speed Host mode, providing up to 480 Mbps. The OCT2224W supports a UTMI+ low-pin interface (ULPI). This interface provides for a low cost means of connecting to off-the-shelf Hi-Speed USB transceivers.

Flash Memory Interface

The OCT2224W supports either ONFI NAND or Serial flash.

DDR3 Memory Subsystem**Direct Memory Access (DMA)**

The DMA controller connects all cores and peripherals to each other and to external memory.

The DMA provides 40 Gbps of bandwidth. This advanced DMA controller provides application-specific modes such as multi-dimensional transfers for matrix processing and high-speed core-to-core and multi-cast transfers.

DDR3 Controller

Support is provided for DDR3 memory devices.

- 32-bit data bus width
- DDR3-667
- Can address up to 2Gbytes total memory
- Typical systems use two 16-bit wide memories.

OCT2224W DC Electrical Characteristics**Absolute Maximum Ratings**

Operation beyond these limits may cause permanent device damage. All parameters representing voltages are measured with respect to ground.

Parameter	Min.	Max.
Core DC supply voltage	-0.5V	1.27V
1.8 V DC supply voltage	-0.5V	2.0V
2.5 V DC supply voltage	-0.2V	3.0V
3.3 V DC supply voltage	-0.5V	4.0V
Storage temperature range	-40°C	+125°C

Recommended Operating Conditions

For normal device operation, adhere to the limits in the table below. Operation beyond these limits may impair the useful life of the device.

Parameter	Min.	Typ.	Max.
Core DC supply voltage		1.0-1.2V	
1.8V I/O DC supply voltage		1.8V	
2.5V I/O DC supply voltage		2.5V	
3.3V I/O DC supply voltage		3.3V	

Ordering Information**OCT22CCZE-PIYV-NN*NNNN**

Field	Description	Options
CC	Number of cores	
Z	Identifies device type	M: Media Processing W: Wireless
E	RoHS lead-free indicator	E: RoHS
P	Package type indicator	B: FCBGA
I	I/O configuration	C: Core Network
Y	Processor	N: None
V	Core Voltage	B: 1.0V device M: 1.06V device T: 1.2V device
NNNNNN	6-digit Project ID number	Assigned by Octasic

Contact your Octasic sales representative for more information.



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